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Reduction of Multiple Triggering in Counting Detectors

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Abstract

We present a scheme for reducing multiple triggering based on a "first-past-the-post" voting circuit interposed between the sensor amplifier/discriminators and the counters in an event counting detector. We are currently designing a proof on concept circuit to implement the scheme and present simulations and preliminary layout to show how this circuit will operate and integrate with the rest of the detector array.

Keywords: Position sensitive detector; microchannel plate; CMOS; multiple triggering

1. Introduction

Multi-anode detectors are conceptually the simplest imaging devices employed with microchannel plates (MCPs). An array of anodes is placed within proximity focus of the rear face of the MCP stack in vacuum or is deposited directly on the rear face of the MCP. Each anode is connected to a conventional electronics channel comprising a charge sensitive amplifier, discriminator and counter. The spatial resolution of the detector is theoretically limited only by the size of the spacing of the anodes. A device has been designed and fabricated using a multi-anode structure on an integrated circuit [1].

In detectors utilising MCPs as an amplification stage, there is always a degree of charge cloud spreading within the MCP stack and also between the MCP stack and the readout device [2]. This charge cloud spreading results in multiple triggering within event counting detectors, leading to degradation of spatial resolution and statistical noise on the resultant spectrum. Although, it is possible to correct for this degradation in software by taking many images with a very short dwell time [3], such an approach is limited in application owing to the low data rate achievable. We therefore present a scheme for reducing such multiple triggering using voting

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circuits interposed between the sensor amplifiers and the counters in an event counting detector [4]. The block diagram of the proposed scheme is presented in Figure 1.

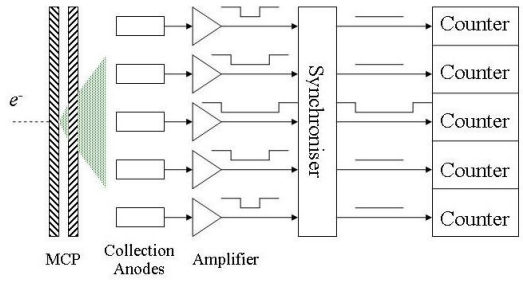

Figure 1 Block diagram of the proposed scheme

The synchronizer is interposed between the outputs of the sensor amplifier/discriminator stage and the counters accumulating the spectrum. The basic principle of operation of the synchronizer relies on the fact that the collection anode nearest the centre of the charge cloud emanating from the MCP will receive more electrons than its neighbors and consequently reach the switching threshold first. The synchronizer is arranged that when a particular channel triggers, its signal is allowed through to the appropriate counter, while at the same time an inhibition signal is generated which prevents the output of the neighboring channels from reaching their counters.

2. Chip configuration

The detector array chip forms the heart of the detector module, imaging the output from the MCP stack. The device effectively forms a one dimensional camera, counting single electrons as they land on the front of the MCP above it.

2.1. Design of collection anodes and charge sensor

The basic sensing element in the detector is a metal electrode connected to a sensitive charge amplifier and discriminator as shown in Figure 2.

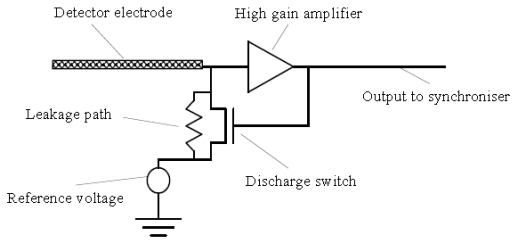

Figure 2 Block diagram of sensor electronics

The anodes, or detector electrodes, collect the electrons emitted by the MCP giving rise to a voltage, which is then detected by the sensors.

The length of the electrode (2mm) is a compromise between the desire to have as large a collection area as possible and the constraints of device size imposed by the semiconductor fabrication process. The width of the electrode is determined by the desired repeat interval of the sensors (25µm) and the minimum gap between structures on the top metal layer imposed by the design rules pertaining to the process used.

The transistor level circuit of the sensor amplifier (high gain) is shown in Figure 3.

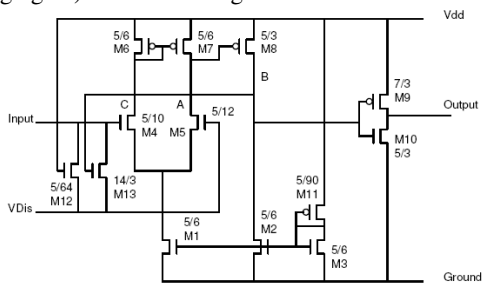

Figure 3 Transistor level sensor amplifier

The long tailed pair is formed M4 & M5, with M6 & M7 as the PMOS active load. Transistor M1 acts as the current source for the long tailed pair. M3 and M11 form a reference current source, which establishes the current flowing down the long tailed pair. Transistors M8 and M2 buffer the output from the long-tailed pair and add more gain. Transistor M12 is a long, thin NMOS device with its gate

connected to VDD and forms the leakage path which brings the input electrode voltage to the reference VDis voltage under quiescent conditions. Transistor M13 is a short, wide device which implements the switch; it is normally kept switched off, as under steady state conditions its gate will be close to 0V. A buffer formed by M9 & M10 inverts the signal from the pre-buffer (M8 & M2) and provides a negative going pulse which is used to trigger counting in the digital acquisition circuitry. A negative going pulse arriving at the input causes M4 to conduct less current. As the current mirror formed by M6 & M7 reduces the current flowing through M5, the voltage at point 'A' will fall. A falling gate voltage on M8 will cause it to conduct more current, causing the voltage at point 'B' to rise. As the voltage at point 'B' rises, transistor M13 will start to conduct, allowing the charge on the input electrode to discharge and the potential to return to VDis, returning the circuit to its quiescent condition. Transistor M12 forms the leakage path, allowing stray charge to leak away from the electrode without triggering the circuit.

2.2. Design of synchroniser

As can be seen from Figure 4, the synchronizer block is formed from a number of 3-input circuits, tiled together such that each 3-input circuit receives an input from its associated pixel and its 2 immediate neighbours. 1- and 2- input 'dummy' circuits are used at the edges of the array to ensure that the parasitic capacitances are kept as equal as possible for all inputs to the synchronizer block. In1 to In192 are the inputs from the sensor amplifiers to the synchronsier. Out1 to Out192 are the outputs from the synchroniser.

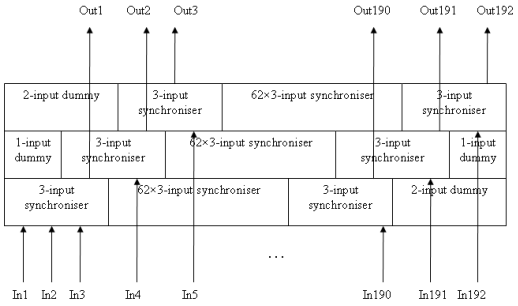

Figure 4 Floor plan of synchroniser

The schematic of single three-input synchroniser is illustrated in Figure 5, in which it can be seen that it is constructed from cross-coupled identical three-input NAND gates. IP is the input from the channel under consideration. IPNa and IPNb are the inhibit inputs supplied by the immediate neighbors of channels. The 3 inputs to the synchronizer pass through the circuit on a metal layer, facilitating tiling the blocks together.

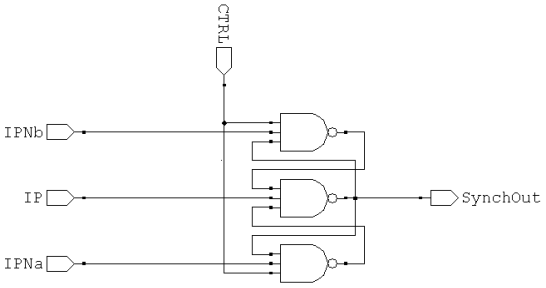

Figure 5 Three-input synchroniser circuit

3. Simulation results

Simulations were performed using the Spice simulator. Simulations were first performed on the circuit after transistor level schematic design and then again after layout using extracted values for parasitic capacitances. The MCP was simulated by assuming that the output was a triangular current pulse with rise time of 150ps and a fall time of 550ps [5]. The peak

amplitude of the current pulse was calculated from the total charge within it (MCP plate gain), the time over which the charge arrived and the distribution of the charge over a number of electrodes. In order to determine the range of MCP gains over which successful operation could be expected, simulations were performed assuming that the adjacent channel received 95% of the charge arriving on the channel of interest. Under these conditions, the transient response of the presented circuit with different plate gains is simulated. As expected, the synchroniser inhibits its neighbors over a wide range of plate gains. The width of the pulse appearing at the synchroniser output was found to depend on the plate gain. The synchroniser was shown to work over a range of plate gains from 2.5×10^5 to 2.5×10^6. The threshold of the sensor amplifier corresponds to a plate gain of 2.5×10^5, below which point no triggering take place. At higher plate gains, the time differential between the synchroniser input and the inhibit signals decreases as shown in Figure 6 until the synchroniser fails to operate. This occurs at a time differential of 76ps, corresponding to a plate gain of 2.5×10^6.

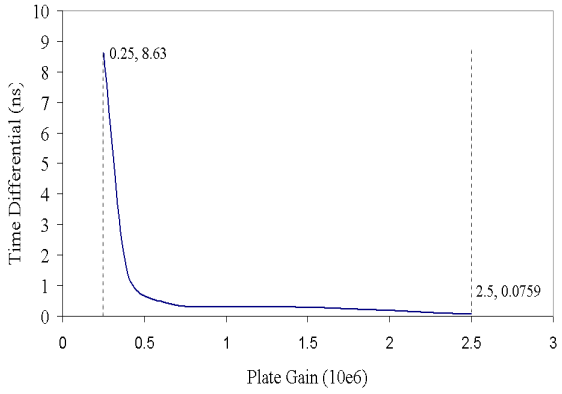

Figure 6 Simulation results of the plate gain versus time differential between the synchroniser input and the inhibit signals

According to the simulation of the circuit, each sensor will dissipate approximately 16μW of power, giving a total static dissipation of 3mW across the array. Digital CMOS circuitry dissipates very little power in a quiescent condition, consuming current only when switching takes place, therefore the dissipation in the digital circuitry will depend upon the speed of incoming charged particles and the speed with which data is clocked out of the array at the end of the reading cycle.

4. Conclusions

A position sensitive detector based on discrete multi-anode technique has been described. The post layout simulation based on AMI 0.5um CMOS process has also been conducted. The simulation results have shown that the proposed detector can detect the range of MCP from 2.5×10^5 to 2.5×10^6.

The final device comprises some 192 3-input synchronisers and 16-bit ripple counters with tri-state outputs, 195 shift register elements, 24 tri-state buffers and other support circuitry. The device count is approximately 130,000 transistors which, when implemented on a 0.5um process, gives an overall silicon die size of 7mm×5mm including the collection anodes.

Acknowledgments

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